Technical Program

2017 International Conference on ReConFigurable Computing and FPGAs

	Sunday, December 3
17:00 - 19:00	Registration

	Monday, December 4
08:30 - 17:30	Registration
08:45 - 09:00	**Opening Session**
09:00 - 10:15	**Keynote #1 - John Watson - Micron, USA**
10:15 - 10:45	Break & Group Photo
10:45-12:50	**Session 1 - General Session**
10:45-11:10	Andreas Engel and Andreas Koch, *Energy-Efficient Reconfiguration of Flash-based FPGAs in Heterogeneous Wireless Sensor Nodes*
11:10-11:35	Christopher Blochwitz, Raphael Klink, Jan Moritz Joseph and Thilo Pionteck. *Contentious Live-Tracing as Debugging Approach on FPGAs*
11:35-12:00	Muhammad Hamdan and Diane T Rover. *VHDL Generator for A High Performance Convolutional Neural Network FPGA-Based Accelerator*
12:00-12:25	Girish Deshpande and Dinesh Bhatia. *Microchannels for Thermal Management in FPGAs*
12:25-12:50	Sizhuo Zhang, Hari Angepat and Derek Chiou. HGum: Messaging Framework for Hardware Accelerators
12:50-14:30	Lunch
14:30 - 16:10	**Session 2 - Reconfigurable Computing for Signal Processing**
14:30-14:55	Éricles Sousa, Alexandru Tanase, Frank Hannig and Jürgen Teich. *A Reconfigurable Memory Architecture for System Integration of Coarse-Grained Reconfigurable Arrays*
14:55-15:20	Metzli Ramirez Martinez, Francisco Sanchez-Fernandez, Philippe Brunet, Sidi Mohammed Senouci and El-Bay Bourennane. *Dynamic management of a partial reconfigurable hardware architecture for pedestrian detection in regions of interest*
15:20-15:45	João Lopes, Diogo Sousa and João Canas Ferreira. *Evaluation of CGRA architecture for real-time processing of biological signals on wearable devices*
15:45-16:10	Hanqing Zeng, Chi Zhang and Viktor Prasanna. *Fast Generation of High Throughput Customized Deep Learning Accelerators on FPGAs*
16:10-16:40	Poster Introductions - Session A
16:40-17:30	**Poster Session A**
19:00 - 21:00	**Welcome Cocktail & Demo Night**

	Tuesday, December 5
08:30 - 17:30	Registration
09:00 - 10:15	**Keynote #2 - Christian Plessl - Paderborn University, Germany**
10:15 - 10:30	Break
10:30-11:45	**Session 3 - Productivity Environments and High Level Languages**
10:30-10:55	Daniel Noronha, Jose Pinilla and Steven Wilton. *Rapid Circuit-Specific Inlining Tuning for FPGA High-Level Synthesis*
10:55-11:20	Lukas Sommer, Julian Oppermann, Jaco Hofmann and Andreas Koch. *Synthesis of Interleaved Multithreaded Accelerators from OpenMP Loops*
11:20-11:45	Pedro Bruel, Alfredo Goldman, Sai Rahul Chalamalasetti and Dejan Milojicic. *Autotuning High-Level Synthesis for FPGAs Using OpenTuner and LegUp*
11:45-12:15	Poster Introductions - Session B
12:15-13:00	**Poster Session B**
13:00-14:30	Lunch

14:30-13:30	**Session 4 - High Performance Reconfigurable Computing**
14:30-14:55	Usman Tariq, Umer Cheema and Fahad Saeed. *Power-Efficient and Highly Scalable Parallel Graph Sampling using FPGAs*
14:55-15:20	Rasha Karakchi, Lothrop Richards and Jason Bakos. *A Dynamically Reconfigurable Automata Processor Overlay*
15:20-15:45	Lucas Bragança, Danilo Almeida, Jose Nacif, Carlos A Hernández-Martínez, Ismael Sánchez-Osorio and Ricardo Ferreira. *Exploring the dynamics of large-scale gene regulatory networks using hardware acceleration on a heterogeneous CPU-FPGA platform*
15:45-16:10	Shijie Zhou, Rajgopal Kannan and Viktor Prasanna. *Accelerating Low Rank Matrix Completion on FPGA*
16:10-16:30	Break
16:30-16:55	**Session 5 - Reconfigurable Computing for Security and Cryptography**
16:55-17:20	Ievgen Kabin, Zoya Dyka, Dan Kreiser and Peter Langendoerfer. *Horizontal Address-Bit DPA against Montgomery kP Implementation*
17:20-17:45	Ahmad Salman, Ahmed Ferozpuri, Ekawat Homsirikamol, Panasayya Yalla, Jens-Peter Kaps and Kris Gaj. *A Scalable ECC Processor Implementation for High-Speed and Lightweight with Side-Channel Countermeasures*
17:45-18:10	Anthony Brandon and Michael Trimarchi. *Trusted Display and Input using Screen Overlays*
18:10-18:35	William Diehl, Abubakr Abdulgadir, Jens-Peter Kaps and Kris Gaj. *Side-channel Resistant Soft Core Processor for Lightweight Block Ciphers*

19:45 - 23:00	**ReConFig Dinner**

	Wednesday, December 5
08:45-11:30	Registration
09:00-10:15	**Session 6 - Reconfigurable Computing for Networks and Communications**
09:00-09:25	Tuncay Soylu, Oguzhan Erdem, Aydın Carus and Edip S. Guner. *Simple CART Based Real-Time Traffic Classification Engine on FPGAs*
09:25-09:50	Qianqiao Chen, Vaibhawa Mishra, Jose Nunez-Yanez and Georgios Zervas. *Synchronizing reconfiguration of coherent functions on disaggregated FPGA resources*
09:50-10:15	Jose Fernando Zazo, Sergio Lopez-Buedo, Mario Ruiz and Gustavo Sutter. *A Single FPGA Architecture for Detecting Heavy Hitters in 100 Gbit/s Ethernet links*
10:15-10:45	Poster Introductions - Session C
10:45-11:30	**Poster Session C**
11:30-12:20	**Session 7 - Multiprocessor Systems and Networks on Chip**
11:30:11:55	Jens Rettkowski and Diana Goehringer. *Application-Specific Processing using High-Level Synthesis for Networks-on-Chip*
11:55-12:20	Pongstorn Maidee, Alireza Kaviani and Kevin Zeng. *LinkBlaze: Efficient Global Data Movement for FPGAs*
12:20:12:50	Poster Introductions - Session D
12:50-13:30	**Poster Session D**
13:30-13:45	**Closing Remarks**

Poster Session A

Tobias Drewes, Jan Moritz Joseph and Thilo Pionteck. *An FPGA-based Prototyping Framework for Networks-on-Chip*

Cesar Torres-Huitzil and Bernard Girau. *Fault tolerance in neural networks: neural design and hardware implementation*

Bernard Girau and Cesar Torres. *Optimal weight storage improves fault tolerance of SOMs*

Umer Farooq, Habib Mehrez and Khurram Bhatti. *Comparison of Direct and Switch-based Inter-FPGA Routing Interconnect for Multi-FPGA Systems*

Takuya Kojima, Naoki Ando, Hayate Okuhara and Hideharu Amano. *Glitch-aware Variable Pipeline Optimization for CGRAs*

Michele Paolino, Sébastien Pinneterre and Daniel Raho. *FPGA virtualization with accelerators overcommitment for Network Function Virtualization*

Poster Session B

Farnoud Farahmand, William Diehl and Kris Gaj. Minerva: Automated Hardware Optimization Tool

Panasayya Yalla and Jens-Peter Kaps. *Evaluation of CAESAR Hardware API for Lightweight Implementations*

Diogo Parrinha and Ricardo Chaves. *Flexible and Low-Cost HSM based on Non-Volatile FPGAs*

Sreeja Chowdhury, Xiaolin Xu, Mark Tehranipoor and Domenic Forte. *Aging Resistant RO PUF with Increased Reliability in FPGA*

Jan Moritz Joseph, Morten Mey, Kristian Ehlers, Christopher Blochwitz, Tobias Winker and Thilo Pionteck. *Design Space Exploration for a Hardware-accelerated Embedded Real-Time Pose Estimation using Vivado HLS*

Andrew Boutros, Brett Grady, Mustafa Abbas and Paul Chow. *Build Fast, Trade Fast: FPGA-based High-Frequency Trading using High-Level Synthesis*

Poster Session C

Benedikt Janßen, Mário Lopes Ferreira, Fatih Korkmaz, Halil Derya, João Canas Ferreira and Michael Huebner. *Towards a Type 0 Hypervisor for Dynamic Reconfigurable Systems*

Siyuan Xu and Benjamin Carrion Schafer. *HW/SW Co-design Experimental Platform using Configurable SoCs*

Paul Rogers, Rajesh Kavasseri and Scott Smith. *An FPGA-in the Loop Approach for HDL Motor Controller Verification*

Jingchi Yang and David Keezer. *Biologically Inspired Hierarchical Structure for Self-Repairing FPGAs*

Tripti Jain, Klaus Schneider and Ankesh Jain. *Optimizing Concentrator Designs by the Half Cleaner Lemma*

Ian Barge and Cristinel Ababei. *H.264 Video Decoder Implemented on FPGAs using 3x3 and 2x2 Networks-on-Chip*

Poster Session D

Mario Ruiz, Gustavo Sutter, Sergio Lopez-Buedo, Jose Fernando Zazo and Jorge Lopez de Vergara. *An FPGA-Based Approach for Packet Deduplication in 100 Gigabit-per-Second Networks*

Hiroki Nakamura, Hirotaka Takayama, Yoshiki Yamaguchi and Taisuke Boku. *Thorough analysis of PCIe Gen3 Communication*
Young Cho and Siddharth Bhragav. *Fine-grained On-line Power Monitoring for Soft Microprocessor based System-on-Chip*
Fredy Augusto Maciel Alves, Peter Jamieson, Lucas Silva, Ricardo Ferreira and José Augusto Nacif. *Designing a Collision Detection Accelerator on a Heterogeneous CPU-FPGA Platform*
Salvador Ibarra-Delgado, Remberto Sandoval-Arechiga, Maria Brox and Manuel Ortiz. *Software Defined Network Controller: a neat solution administration for reconfigurable multi-core NoC*
Claudio Rubattu, Francesca Palumbo and Maxime Pelcat. *Adaptive Software-Augmented Hardware Reconfiguration with Dataflow Design Automation*