

Technical Program

2018 International Conference on ReConFIGurable Computing and FPGAs

Sunday, December 2

09:00 - 18:00

Xilinx's Workshop

17:00 - 19:00

Registration

Monday, December 3

08:00 - 18:00

Registration

08:45 - 09:00

Opening

09:00 - 10:10

Keynote #1 - "FPGAs at HyperScale -- The Past, Present, and Future of the Reconfigurable Cloud" by Andrew Putnam, Microsoft Research, USA

10:10 - 10:40

Break & Group Photo

10:40 - 12:45

Session 1: Reconfiguration architectures - Chair: Peter Athanas

10:40 - 11:05

Rafael Zamacola, Alberto García Martínez, Javier Mora, Andrés Otero and Eduardo de La Torre. *IMPRESS: Automated Tool for the Implementation of Highly Flexible Partial Reconfigurable Systems with Xilinx Vivado*

10:05 - 11:30

Tiziana Fanni, Alfonso Rodriguez, Carlo Sau, Leonardo Suriano, Francesca Palumbo, Luigi Raffo and Eduardo de la Torre. *Multi-Grain Reconfiguration for Advanced Adaptivity in Cyber-Physical Systems*

11:30 - 11:55

Gökhan Akgün, Habib ul Hasan Khan, Mahmoud Ahmed Elshimy and Diana Göhringer. *Dynamic tunable and reconfigurable hardware controller with EKF-based state reconstruction through FPGA-in the loop*

11:55 - 12:20

Dillon Huff and Pat Hanrahan. *Using Runtime Circuit Specialization to Accelerate Simulations of Reconfigurable Architectures*

12:20 - 12:45

Arpit Soni, Yoon Kah Leow and Ali Akoglu. *Post-Routing Analytical Wirelength Model for Homogeneous FPGA Architectures*

12:45 - 14:30

Lunch

14:30 - 16:10

Session 2: Security, Cryptography, Fault Tolerance, and High Assurance - Chair: Aydin Aysu

14:30 - 14:55

Ahmed Ferozpuri and Kris Gaj. *High-speed FPGA Implementation of the NIST Round 1 Rainbow Signature Scheme*

14:55 - 15:20	Michael Tempelmeier, Jens-Peter Kaps and Georg Sigl. <i>Experimental Power and Performance Evaluation of CAESAR Hardware Finalists</i>
15:20 - 15:45	Muhammad Abdul Wahab, Pascal Cotret, Mounir Nasr Allah, Guillaume Hiet, Vianney Lapotre, Guy Gogniat and Arnab Kumar Biswas. <i>A small and adaptive coprocessor for information flow tracking in ARM SoCs</i>
15:45 - 16:10	Daniel Ziener and Jutta Pirkel. <i>Configuration Tampering of BRAM-based AES Implementations on FPGAs</i>
16:10 - 16:30	Break
16:30 - 17:25	Session 3: Design and acceleration of applications - Chair: Daniel Ziener
16:30 - 16:55	John McGlone, Paolo Palazzari and Jean-Baptiste Leclere. <i>Accelerating Key In-memory Database Functionality with FPGA Technology</i>
16:55 - 17:20	Alan Ehret, Mihailo Isakov and Michel A. Kinsky. <i>Towards a Generalized Reconfigurable Agent Based Architecture: Stock Market Simulation Acceleration</i>
17:20 - 17:55	Paulina M. Fusiara, Gijs Schoonderbeek, Johan Pragt, Leon Hiemstra, Menno Schuil, Sjouke Kuindersma and Grant A. Hampson. <i>Design and Fabrication of Full Board Direct Liquid Cooling Heat Sink for Densely Packed FPGA Processing Boards</i>
19:00 - 21:00	Welcome Cocktail & Demo Night
	Tuesday, December 4
08:30 - 18:30	Registration
09:00 - 10:10	Keynote #2 - "Just in Time Mission Composition: Tipping the Assurance Balance in Cyberspace" by Erich Devendorf, Air Force Research Laboratory, USA
10:10 - 10:30	Break
10:30 - 13:00	Session 4: Machine Learning - Chair: Tinoosh Mohsenin
10:30 - 10:55	Ali Jafari, Morteza Hosseini, Houman Homayoun and Tinoosh Mohsenin. <i>A Scalable and Low Power DCNN for Multimodal Data Classification</i>
10:55 - 11:20	Weiyi Sun, Hanqing Zeng, Yi-Hua Edward Yang and Viktor Prasanna. <i>Throughput-Optimized Frequency Domain CNN with Fixed-Point Quantization on FPGA</i>
11:20 - 11:45	Ahmed Abdelsalam, Felix Boulet, Gabriel Demers, J. M. Pierre Langlois and Farida Cheriet. <i>An Efficient FPGA-based Overlay Inference Architecture for Fully Connected DNNs</i>

11:45 - 12:10	Takashi Takemoto, Mertig Normann, Masato Hayashi, Saki Susa-Tanaka, Hiroshi Teramoto, Atsuyoshi Nakamura, Ichigaku Takigawa, Shin-Ichi Minato, Tamiki Komatsuzaki and Masanao Yamaoka. <i>FPGA-Based QBoost with Large-Scale Annealing Processor and Accelerated Hyperparameter Search</i>
12:10 - 12:30	Poster Introductions - Session A
12:30 - 13:00	Poster Session A - 4 posters
13:00 - 14:30	Lunch
14:30 - 15:40	Keynote #3 - "Adaptable Intelligent Computing from Edge to Cloud" by Hugo A. Andrade, Director, Xilinx University Program, USA
15:40 - 15:45	Short Break
15:45 - 16:35	Session 5: High Performance Computing Systems and Applications - Chair: Travis Haroldsen
15:45 - 16:10	Gustavo Sutter, Mario Ruiz, Sergio López-Buedo and Gustavo Alonso. <i>FPGA-based TCP/IP Checksum Offloading Engine for 100 Gbps Networks</i>
16:10 - 16:35	Matthew Cauwels, Joseph Zambreno and Phillip H. Jones. <i>HW/SW Configurable LQG Controller using a Sequential Discrete Kalman Filter</i>
16:35 - 16:50	Break
16:50 - 18:30	Session 6: Productivity Environments and High Level Languages - Chair: Eduardo de la Torre
16:50 - 17:15	Zheming Jin and Hal Finkel. <i>Evaluating Floating-point Intensive Applications on OpenCL FPGA Platforms: A Case Study on the SimpleMOC Kernel</i>
17:15 - 17:40	Mohamed Hassan, Ahmed Helal, Peter Athanas, Wu-Chun Feng and Yasser Hanafy. <i>Exploring FPGA-specific Optimizations for Irregular OpenCL Applications</i>
17:40 - 18:05	Morgan McColl, Vlad Estivill-Castro and Rene Hexel. <i>High-Level Executable Models of Reactive Real-Time Systems with Logic-Labelled Finite-State Machines and FPGAs</i>
18:05 - 18:30	Franz-Josef Streit, Martin Letras, Stefan Wildermann, Benjamin Hackenberg, Joachim Falk, Andreas Becher and Jürgen Teich. <i>Model-Based Design Automation of Hardware/Software Co-Designs for Xilinx Zynq PSoCs</i>
20:00 - 22:30	ReConFig Dinner

Wednesday, December 5	
09:00 - 12:00	Registration
09:00 - 10:15	Session 7: Real Time Image and Signal Processing - Chair: Jin Zheming
09:00 - 09:25	Norbert Abel, William Kamp and Gianni Comoretto. <i>Complex Multiply Accumulate Cells for the Square Kilometre Array Correlators</i>
09:25 - 09:50	Ryo Kamasaka, Yuichiro Shibata and Kiyoshi Oguri. <i>An FPGA-oriented Graph Cut Algorithm for Accelerating Stereo Vision</i>
09:50 - 10:15	Joe Avey, Phillip H. Jones and Joseph Zambreno. <i>An FPGA-based Hardware Accelerator for Iris Segmentation</i>
10:15 - 10:40	Poster Introductions - Session B
10:40 - 11:10	Break - Poster Session B - 4 posters
11:10 - 12:00	Session 8: Multiprocessor and Heterogeneous Architectures - Chair: William Harrison
11:10 - 11:35	Shuai Xie, Zhongyuan Zhao, Weiguang Sheng, Qin Wang and Zhigang Mao. <i>MBSS: A General Paradigm for Static Schedule for Nested Loops with Dynamic Loop Boundary on CGRAs</i>
11:35 - 12:00	Kris Heid and Christian Hochberger. <i>AutoStreams: Fully Automatic parallelization of Legacy Embedded Applications with Soft-Core MPSoCs</i>
12:00 - 12:30	Poster Introductions - Session C
12:30 - 13:00	Break - Poster Session C - 4 posters
13:00 - 13:10	Closing Remarks
13:10 - 14:00	Lunch
14:00 - 18:00	Digilent's Workshop

Poster Session A

Takeharu Ikezoe, Hideharu Amano, Junya Akaike, Kudo Masaru, Kimiyoshi Usami, Keizo Hiraga, Yusuke Shuto and Kojiro Yagami. *A Coarse Grained-Reconfigurable Accelerator with energy efficient MTJ-based Non-volatile Flip-flops*

Safdar Mahmood, Pavel Shydlouski and Michael Huebner. *An Application Specific Framework for HLS-based FPGA Design of Articulated Robot Inverse Kinematics*

Kalindu Herath, Alok Prakash, Jiang Guiyuan and Thambipillai Srikanthan. *Ant Colony Optimization based Module Footprint Selection and Placement for Lowering Power in Large FPGA Designs*

Hsin-Yu Ting, Ardalan Amiri Sani and Eli Bozorgzadeh. *System Services for Reconfigurable Hardware Acceleration in Mobile Devices*

Poster Session B

Philipp Käsgen, Markus Weinhardt and Christian Hochberger. *A Coarse-Grained Reconfigurable Array for High-Performance Computing Applications*

Sourya Dey, Diandian Chen, Zongyang Li, Souvik Kundu, Kuan-Wen Huang, Keith Chugg and Peter Beerel. *A Highly Parallel FPGA Implementation of Sparse Neural Network Training*

William Harrison and Gerard Allwein. *Language Abstractions for Hardware-based Control-Flow Integrity Monitoring*

Zoya Dyka, Dan Kreiser, Ievgen Kabin and Peter Langendoerfer. *Flexible FPGA ECDSA Design with a Field Multiplier Inherently Resistant against HCCA*

Poster Session C

Ievgen Kabin, Dan Kreiser, Zoya Dyka and Peter Langendoerfer. *FPGA Implementation of ECC: Low-Cost Countermeasure against Horizontal Bus and Address-Bit SCA*

Paul Sathre, Ahmed Helal and Wu-Chun Feng. *A Composable Workflow for Productive Heterogeneous Computing on FPGAs via Whole-Program Analysis and Transformation*

Lester Kalms, Hassan Ibrahim and Diana Goehringer. *Full-HD Accelerated and Embedded Feature Detection Video System with 63fps using ORB for FREAK*

Yuta Tokusashi, Hiroki Matsutani and Noa Zilberman. *LaKe: The Power of In-Network Computing*