Preliminary Technical Program

2018 International Conference on ReConFigurable Computing and FPGAs

	Sunday, December 2
09:00 - 18:00	**Xilinx's Workshop**
17:00 - 19:00	Registration
	Monday, December 3
08:00 - 18:00	Registration
08:45 - 09:00	**Opening**
09:00 - 10:10	**Keynote #1**
10:10 - 10:40	Break & Group Photo
10:40 - 12:45	**Session 1: Reconfiguration architectures**
10:40 - 11:05	Rafael Zamacola, Alberto García Martínez, Javier Mora, Andrés Otero and Eduardo de La Torre. *IMPRESS: Automated Tool for the Implementation of Higly Flexible Partial Reconfigurable Systems with Xilinx Vivado*
10:05 - 11:30	Tiziana Fanni, Alfonso Rodriguez, Carlo Sau, Leonardo Suriano, Francesca Palumbo, Luigi Raffo and Eduardo de la Torre. *Multi-Grain Reconfiguration for Advanced Adaptivity in Cyber-Physical Systems*
11:30 - 11:55	Gökhan Akgün, Habib ul Hasan Khan, Mahmoud Ahmed Elshimy and Diana Göhringer. *Dynamic tunable and reconfigurable hardware controller with EKF-based state reconstruction through FPGA-in the loop*
11:55 - 12:20	Dillon Huff and Pat Hanrahan. *Using Runtime Circuit Specialization to Accelerate Simulations of Reconfigurable Architectures*
12:20 - 12:45	Arpit Soni, Yoon Kah Leow and Ali Akoglu. *Post-Routing Analytical Wirelength Model for Homogeneous FPGA Architectures*
12:45 - 14:30	Lunch
14:30 - 16:10	**Session 2: Security, Cryptography, Fault Tolerance, and High Assurance**
14:30 - 14:55	Ahmed Ferozpuri and Kris Gaj. *High-speed FPGA Implementation of the NIST Round 1 Rainbow Signature Scheme*
14:55 - 15:20	Michael Tempelmeier, Jens-Peter Kaps and Georg Sigl. *Experimental Power and Performance Evaluation of CAESAR Hardware Finalists*

15:20 - 15:45	Muhammad Abdul Wahab, Pascal Cotret, Mounir Nasr Allah, Guillaume Hiet, Vianney Lapotre, Guy Gogniat and Arnab Kumar Biswas. *A small and adaptive coprocessor for information flow tracking in ARM SoCs*
15:45 - 16:10	Daniel Ziener and Jutta Pirkl. *Configuration Tampering of BRAM-based AES Implementations on FPGAs*
16:10 - 16:30	Break
16:30 - 17:25	**Session 3: Design and acceleration of applications**
16:30 - 16:55	John McGlone, Paolo Palazzari and Jean-Babtiste Leclere. *Accelerating Key In-memory Database Functionality with FPGA Technology*
16:55 - 17:20	Alan Ehret, Mihailo Isakov and Michel A. Kinsy. *Towards a Generalized Reconfigurable Agent Based Architecture: Stock Market Simulation Acceleration*
17:20 - 17:55	Paulina M. Fusiara, Gijs Schoonderbeek, Johan Pragt, Leon Hiemstra, Menno Schuil, Sjouke Kuindersma and Grant A. Hampson. *Design and Fabrication of Full Board Direct Liquid Cooling Heat Sink for Densely Packed FPGA Processing Boards*
19:00 - 21:00	**Welcome Cocktail & Demo Night**

	Tuesday, December 4
08:30 - 18:30	Registration
09:00 - 10:10	**Keynote #2**
10:10 - 10:30	Break
10:30 - 13:00	**Session 4: Machine Learning**
10:30 - 10:55	Ali Jafari, Morteza Hosseini, Houman Homayoun and Tinoosh Mohsenin. A Scalable and Low Power DCNN for Multimodal Data Classification
10:55 - 11:20	Weiyi Sun, Hanqing Zeng, Yi-Hua Edward Yang and Viktor Prasanna. Throughput-Optimized Frequency Domain CNN with Fixed-Point Quantization on FPGA
11:20 - 11:45	8Ahmed Abdelsalam, Felix Boulet, Gabriel Demers, J. M. Pierre Langlois and Farida Cheriet. *An Efficient FPGA-based Overlay Inference Architecture for Fully Connected DNNs*

11:45 - 12:10	22Takashi Takemoto, Mertig Normann, Masato Hayashi, Saki Susa-Tanaka, Hiroshi Teramoto, Atsuyoshi Nakamura, Ichigaku Takigawa, Shin-Ichi Minato, Tamiki Komatsuzaki and Masanao Yamaoka. *FPGA-Based QBoost with Large-Scale Annealing Processor and Accelerated Hyperparameter Search*
12:10 - 12:30	Poster Introductions - Session A
12:30 - 13:00	**Poster Session A - 4 posters**
13:00 - 14:30	Lunch
14:30 - 15:40	**Keynote #3**
15:40 - 15:45	Short Break
15:45 - 16:35	**Session 5: High Performance Computing Systems and Applications**
15:45 - 16:10	Gustavo Sutter, Mario Ruiz, Sergio López-Buedo and Gustavo Alonso. FPGA-based TCP/IP Checksum Offloading Engine for 100 Gbps Networks
16:10 - 16:35	Matthew Cauwels, Joseph Zambreno and Phillip H. Jones. *HW/SW Configurable LQG Controller using a Sequential Discrete Kalman Filter*
16:35 - 16:50	Break
16:50 - 18:30	**Session 6: Productivity Environments and High Level Languages**
16:50 - 17:15	Zheming Jin and Hal Finkel. *Evaluating Floating-point Intensive Applications on OpenCL FPGA Platforms: A Case Study on the SimpleMOC Kernel*
17:15 - 17:40	Mohamed Hassan, Ahmed Helal, Peter Athanas, Wu-Chun Feng and Yasser Hanafy. *Exploring FPGA-specific Optimizations for Irregular OpenCL Applications*
17:40 - 18:05	Morgan McColl, Vlad Estivill-Castro and Rene Hexel. *High-Level Executable Models of Reactive Real-Time Systems with Logic-Labelled Finite-State Machines and FPGAs*
18:05 - 18:30	Franz-Josef Streit, Martin Letras, Stefan Wildermann, Benjamin Hackenberg, Joachim Falk, Andreas Becher and Jürgen Teich. *Model-Based Design Automation of Hardware/Software Co-Designs for Xilinx Zynq PSoCs*
20:00 - 22:30	**ReConFig Dinner**

	Wednesday, December 5
09:00 - 12:00	Registration
09:00 - 10:15	**Session 7: Real Time Image and Signal Processing**
09:00 - 09:25	Norbert Abel, William Kamp and Gianni Comoretto. *Complex Multiply Accumulate Cells for the Square Kilometre Array Correlators*
09:25 - 09:50	Ryo Kamasaka, Yuichiro Shibata and Kiyoshi Oguri. *An FPGA-oriented Graph Cut Algorithm for Accelerating Stereo Vision*
09:50 - 10:15	Joe Avey, Phillip H. Jones and Joseph Zambreno. *An FPGA-based Hardware Accelerator for Iris Segmentation*
10:15 - 10:40	Poster Introductions - Session B
10:40 - 11:10	**Break - Poster Session B - 5 posters**
11:10 - 12:00	**Session 8: Multiprocessor and Heterogeneous Architectures**
11:10 - 11:35	Shuai Xie, Zhongyuan Zhao, Weiguang Sheng, Qin Wang and Zhigang Mao. *MBSS:A General Paradigm for Static Schedule for Nested Loops with Dynamic Loop Boundary on CGRAs*
11:35 - 12:00	Kris Heid and Christian Hochberger. *AutoStreams: Fully Automatic parallelization of Legacy Embedded Applications with Soft-Core MPSoCs*
12:00 - 12:30	Poster Introductions - Session C
12:30 - 13:00	**Break - Poster Session C - 6 posters**
13:00 - 13:10	**Closing Remarks**
13:10 - 14:00	Lunch
14:00 - 18:00	**Digilent's Workshop**

Poster Session A
Takeharu Ikezoe, Hideharu Amano, Junya Akaike, Kudo Masaru, Kimiyoshi Usami, Keizo Hiraga, Yusuke Shuto and Kojiro Yagami. *A Coarse Grained-Reconfigurable Accelerator with energy efficient MTJ-based Non-volatile Flip-flops*
Safdar Mahmood, Pavel Shydlouski and Michael Huebner. *An Application Specific Framework for HLS-based FPGA Design of Articulated Robot Inverse Kinematics*
Kalindu Herath, Alok Prakash, Jiang Guiyuan and Thambipillai Srikanthan. *Ant Colony Optimization based Module Footprint Selection and Placement for Lowering Power in Large FPGA Designs*
Hsin-Yu Ting, Ardalan Amiri Sani and Eli Bozorgzadeh. *System Services for Reconfigurable Hardware Acceleration in Mobile Devices*

Poster Session B
Philipp Käsgen, Markus Weinhardt and Christian Hochberger. *A Coarse-Grained Reconfigurable Array for High-Performance Computing Applications*
Sourya Dey, Diandian Chen, Zongyang Li, Souvik Kundu, Kuan-Wen Huang, Keith Chugg and Peter Beerel. *A Highly Parallel FPGA Implementation of Sparse Neural Network Training*
William Harrison and Gerard Allwein. *Language Abstractions for Hardware-based Control-Flow Integrity Monitoring*
Zoya Dyka, Dan Kreiser, Ievgen Kabin and Peter Langendoerfer. *Flexible FPGA ECDSA Design with a Field Multiplier Inherently Resistant against HCCA*
Ievgen Kabin, Dan Kreiser, Zoya Dyka and Peter Langendoerfer. *FPGA Implementation of ECC: Low-Cost Countermeasure against Horizontal Bus and Address-Bit SCA*

Poster Session C
Paul Sathre, Ahmed Helal and Wu-Chun Feng. *A Composable Workflow for Productive Heterogeneous Computing on FPGAs via Whole-Program Analysis and Transformation*
Lester Kalms, Hassan Ibrahim and Diana Goehringer. *Full-HD Accelerated and Embedded Feature Detection Video System with 63fps using ORB for FREAK*

Yuta Tokusashi, Hiroki Matsutani and Noa Zilberman. *LaKe: The Power of In-Network Computing*
Dilshan Kumarathunga, Omega Gamage, Asitha Samarasinghe, Nipuna Saranga, Ranga Rodrigo and Ajith Pasqual. *VLIW Based Runtime Reconfigurable Machine Vision Coprocessor Architecture for Edge Processing*